NONLINEAR ANALYSIS OF $f_0/2$ LOOP OSCILLATION OF HIGH POWER AMPLIFIERS

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ABSTRACT

A novel nonlinear analysis of high power amplifier instability has been developed. This analysis method deals with a loop oscillation and presents the conditions for oscillation under large-signal operation by taking account of a mixing effect of FETs. Applying this analysis method to the high power amplifier instability that an output power decreases at some compression point where an $f_0/2$-wave is observed, it has been found that this instability is caused by an $f_0/2$ loop oscillation. In addition, it has been verified by analysis and measurement that the oscillation can be removed by employing an isolation resistor in a closed loop circuit.

INTRODUCTION

In recent years, a number of solid-state power amplifiers have been reported in applications to microwave communication and measurement systems [1],[2],[3]. In the design of high power amplifiers, several FETs are connected in parallel to achieve high output power. In these amplifiers, the phenomenon that an output power decreases at some compression point can be observed in some cases, where an $f_0/2$-wave is observed. In the design of microwave amplifiers, a K-factor has been used as a method for analyzing circuit stability [4]. However, it cannot predict an oscillation in a closed loop circuit [5]. In 1988, R.G.Freitag et al. analyzed the odd mode oscillation in a closed loop circuit and applied this method to the stability analysis of power amplifiers [6]. In this analysis, however, the conditions for oscillation have not been clearly established. We presented a linear analysis method of the loop oscillation in a closed loop circuit and clearly stated the conditions for oscillation in 1994 [7]. In this paper, we introduce a novel nonlinear analysis method and present the conditions for oscillation under large-signal operation by taking account of a mixing effect of FETs. Applying this analysis method to the high power amplifier instability that an output power decreases at some compression point where an $f_0/2$-wave is observed, it has been found that this instability is caused by an $f_0/2$-wave loop oscillation. In addition, it has been verified that the oscillation can be removed by employing an isolation resistor in a closed loop circuit.

PHENOMENON AND MECHANISM OF INSTABILITY DUE TO $f_0/2$ LOOP OSCILLATION

A phenomenon that an output power decreases at some compression point is shown in Fig.1. As the input power increases, the output power decreases at some compression point, where an $f_0/2$-wave is observed.

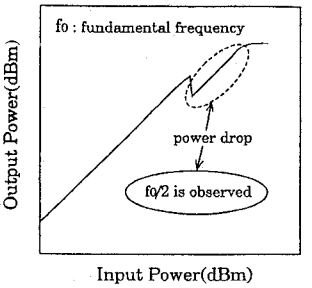

Fig.1 Phenomenon that an output power decreases at some compression point

A mechanism for generating the $f_0/2$-wave can be

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explained by taking into account a mixing of f_0 and $f_0/2$ and an loop oscillation for the $f_0/2$-wave in a closed loop circuit, which is shown in Fig.2. In Fig.2, two FETs are combined in parallel. When the conditions of loop oscillation for an $f_0/2$-wave are satisfied, the $f_0/2$-wave is observed and the output power of an f_0-wave decreases.

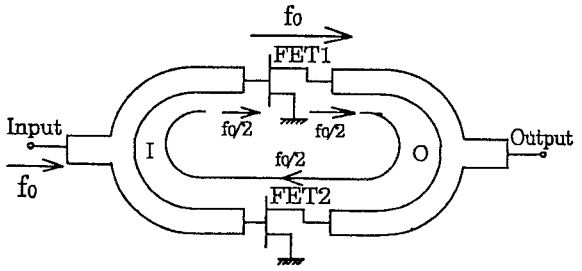
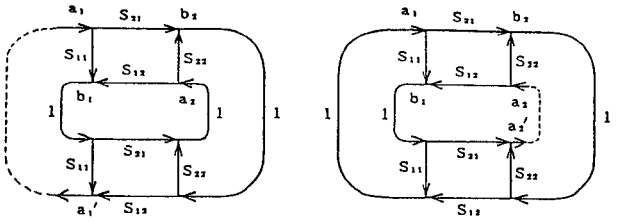


Fig.2 Mechanism for generating the $f_0/2$-wave

The conditions of an $f_0/2$ loop oscillation can be calculated by taking account of traveling-waves which propagate around a closed loop circuit. Signal flows for the signal injected from the input and output sides in a closed loop circuit are shown in Figs.3(a) and (b), respectively, where a_1, a_1', a_2, a_2', b_1 and b_2 are input and output traveling-wave signals, and Sij are S-parameters of the $f_0/2$-wave.



(a) Input side (b) Output side

Fig.3 Signal flows in a closed loop circuit

A loop oscillation is generated when either following condition A or B is satisfied.

[condition A] $|a_1'/a_1| \geqq 1$ and $\angle(a_1'/a_1) = 2m\pi$ (1)

[condition B] $|a_2'/a_2| \geqq 1$ and $\angle(a_2'/a_2) = 2n\pi$ (2)

The conditions of a continuous loop oscillation are $a_1'=a_1$ or $a_2'=a_2$.

NONLINEAR ANALYSIS OF INSTABILITY DUE TO $f_0/2$-WAVE LOOP OSCILLATION

Schematic diagrams for calculating the conditions for an $f_0/2$ loop oscillation of the amplifier with two FETs in parallel is shown in Fig.4. In calculation of the conditions of oscillation for the input or output side, the schematic diagram shown in Fig.4(a) or 4(b) is used, respectively. In Fig.4, two types of ideal band-pass filters for selecting an f_0- or $f_0/2$-wave and ideal circulators for separating incident waves (a_1, a_2) and reflected waves (a_1', a_2') are employed. The two FETs are matched to $R_0 = 50\ \Omega$ through input and output matching circuits for the frequency of f_0 and are terminated by $R_0 = 50\ \Omega$ for the frequency of $f_0/2$. The conditions for an $f_0/2$ loop oscillation (a_1'/a_1 or a_2'/a_2) dependent on the input power of an f_0-wave can be calculated by using a harmonic balance simulation. An accurate modeling and calculation of the $f_0/2$ loop oscillation becomes possible with the use of the schematic diagram shown in Fig.4 because a mixing effect of f_0- and $f_0/2$-waves can be taken into account, which has not been considered in Ref.(7).

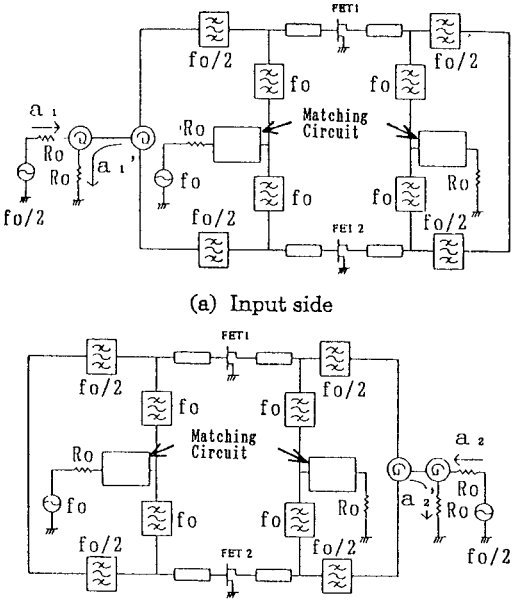


Fig.4 Schematic diagram for calculating the conditions for an $f_0/2$ loop oscillation of the amplifier with two FETs in parallel

AMPLIFIER DESIGN

In order to verify the $f_0/2$ loop oscillation described in the previous chapter, an amplifier was designed to

show high power and high power at a fundamental frequency of f_0 in addition to having a loop gain for $f_0/2$. The amplifier was designed in accordance with the following approaches:

(1) Two FETs are connected in parallel.

(2) The input matching network is designed for high gain and output matching network for high power at f_0.

(3) The conditions for oscillation described in Eqs.(1) and (2) are satisfied at $f_0/2$.

A schematic diagram of the amplifier is shown in Fig.5. Two FETs having a gate periphery of 3 mm are employed. The fundamental frequency (f_0) is around 4 GHz. The input and output matching networks employs quarter-wavelength impedance transformers

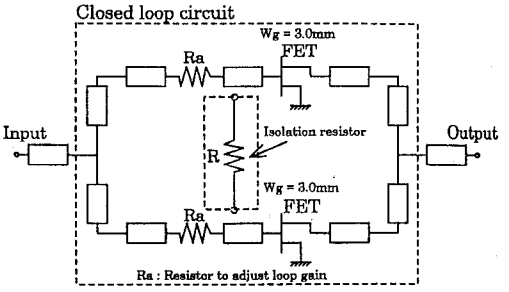
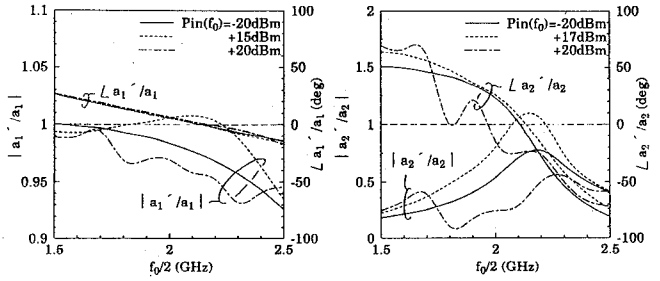


Fig.5 Schematic diagram of the amplifier

for matching and series resistors for adjusting a loop gain. The calculated linear gain is greater than 9 dB for 3 to 5 GHz. The loop gain $|a_1'/a_1|$ and phase $\angle(a_1'/a_1)$ as a function of the input power level (P_{in}) are calculated and plotted in Fig.6(a) for the input side and in Fig.6(b) for the output side, respectively. It is noted in Fig.6 that the conditions for oscillation are satisfied at $f_0/2$ = 2.14 GHz and P_{in} = +15 dBm for the input side and at $f_0/2$ = 2.13 GHz and P_{in} = +17 dBm for the output side.



(a) Input side (b) Output side

Fig.6 Loop gain $|a_1'/a_1|$ and phase $\angle(a_1'/a_1)$ as a function of the input power level (P_{in})

EXPERIMENTAL RESULTS

The measured output power and power-added efficiency of the amplifier for f_0=4.7GHz are shown in Fig.7. It is observed that the output power started to decrease at around +16.5 dBm of input power and stopped at around +22.5 dBm. The measured output power spectra of the amplifier at points a and b of Fig.7 are shown in Figs.8(a) and (b), respectively. At point a, only the fundamental wave (f_0) and second harmonic wave ($2f_0$) are observed. On the other hand, at point b, $f_0/2$ and $3f_0/2$ in conjunction with f_0 and $2f_0$ are observed. In comparison with the calculated results, both the frequency and input power level for oscillation become higher and wider. This is probably due to some errors in the model parameters of FETs.

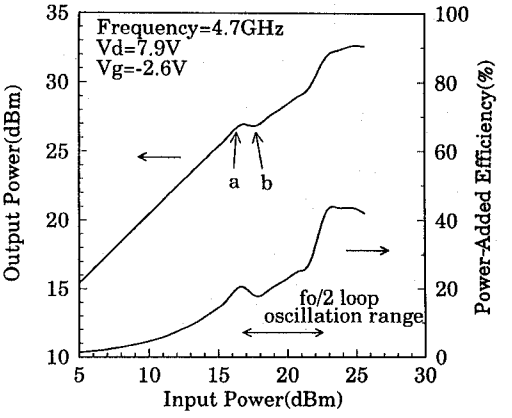
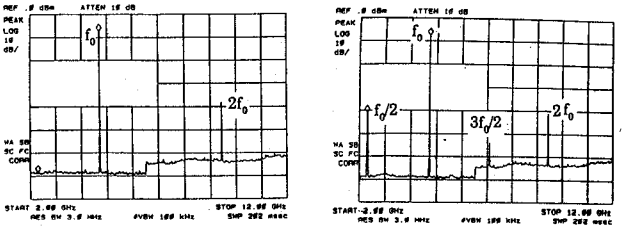


Fig.7 Measured output power and power-added efficiency of the amplifier

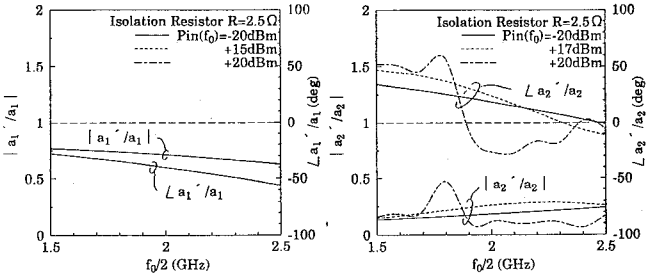


(a) Point a (b) Point b

Fig.8 Measured output power spectra of the amplifier

To remove the $f_0/2$ loop oscillation, we employed an isolation resistor (R) between two FETs shown in Fig.5. The calculated loop gain and phase of the amplifier

employing an isolation resistor (R = 2.5 Ω) are shown in Fig.9. It is clearly shown in Fig.9 that the loop gains of $|a_1'/a_1|<1$ and $|a_2'/a_2|<1$ are obtained. The measured output power and power-added efficiency are shown in Fig.10. The decrease of output power at some compression point was completely removed.



(a) Input side (b) Output side

Fig.9 Calculated loop gain and phase of the amplifier employing an isolation resistor

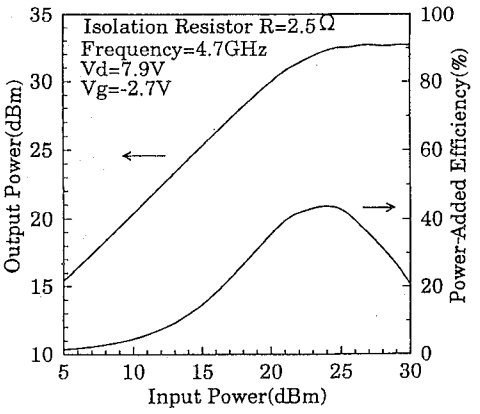


Fig.10 Measured output power and power-added efficiency

CONCLUSION

A novel analysis method of high power amplifier instability has been developed. In this analysis, the conditions for a loop oscillation under large-signal operation has been obtained by taking account of a mixing effect of FETs. Applying this analysis method to the high power amplifier instability that an output power decreases at some compression point where an $f_0/2$-wave is observed, it has been found that this instability is caused by an $f_0/2$ loop oscillation. In addition, it has been verified by analysis and measurement that the oscillation can be removed by employing an isolation resistor in a closed loop circuit. This analysis method will be a candidate for analyzing an instability related to the loop oscillation of high power amplifiers.

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